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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/627,381	07/28/2000	GURTEJ SANDHU	11675.76.1.1	2473

7590 10/02/2002

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EXAMINER
QUACH, TUAN N

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/627,381	SANDHU ET AL.	
	Examiner	Art Unit	
	Tuan Quach	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-10, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. taken with both Jeng and Shih et al.

Kodera et al. teach patterning of conductor including an additional layer thereon to form adjacent conductive lines, depositing dielectric layer thereon and planarizing the dielectric layer. The removal of the additional layer if desired is also shown. See Figs. 30A-30B, 33A-33J, column 28 lines 38-68, column 31 line 33 to column 32 line 68. The additional layer employed is not limited to non-conductive materials and is presumed to

be conductive and further encompasses conductive materials such as polysilicon, carbon, titanium nitride and their interchangeability and selection of suitable conventional conductive materials would have been within the purview of one skilled in the art. Kodera et al. lack anticipation primarily in that the dielectric is not explicitly recited to be less than 3.6 or to be PTFE.

Jeng '493 teaches the use of low dielectric constant material, e.g., organic polymer such as polytetrafluoroethylene, column 3 lines 48-52, between interconnect lines to reduce line-to-line capacitance, crosstalk, power dissipation, RC time delay. The provision of the material between the conductive lines followed by etchback is also taught. Subsequent dielectric deposition and planarization is also taught. See column 1 line 30 to column 2 line 15, column 3 line 29 to column 5 line 43.

Jeng '303 also teach the problem of RC delayer, power dissipation, crossstalk due to dielectric having high dielectric constant, e.g., column 1 lines 37-63, and further teach the use of low k dielectric between the stacks, e.g., as in Fig. 8-10, column 2 lines 37-38, column 3 lines 12-47, column 4 lines 48-61.

Shih et al. teach spaces 24 between conductor pattern 15 extending below a lower surface of the conductor 15. The advantages include the removal of any residues between adjacent electrodes thereby preventing shortage. See the abstract, Figs. 6-7, column 1 line 33 to column 2 line 2, column 3 lines 38-41. The prior art process of provision of spaces below the wiring, e.g., 18, is also shown in Fig. 1C column 1 lines 42-61.

It would have been obvious to one skilled in the art at the time the invention was made in practicing the Kodera et al. process to have employed low dielectric constant materials including below 3.6 such as polytetrafluoroethylene between interconnect lines as taught by Jeng '493 and 'Jeng '303 since such is conventional and advantageous as evidenced by Jeng. Etchback for planarization is conventional as evidenced by Jeng and further is a well-known alternative to chemical mechanical polishing and as such would have been obvious. The planarization of the upper insulating is well known in the art as evidenced by Jeng and enables a planarized top insulating surface to be obtained. The use of various alternative conductive materials, e.g., in claim 10, is well within the purview of one skilled in the art and as such would have been obvious. It would have been further obvious to one skilled in the art in practicing the above invention to have included effected the etching patterned the adjacent wiring the space below the lower surface of adjacent wirings since such is conventional in the art as evidenced in Shih et al. to remove residue or nodules thereby preventing shortage between adjacent electrodes. The dielectric having lower surface below lower surface of adjacent conductive lines would follow when such overetch is employed as suggested by Shih et al.

Regarding the fringe capacitance recited in certain claims, e.g., claims 35-38, to the extent such is required to any specified or sufficient extent, such would be realized or result when the dielectric is situated above or below the surface of the adjacent conductive lines and further would follow when low dielectric constant material is employed.

Claims 11-35, 37, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. taken with both Jeng and Shih et al.

Kodera et al. teach patterning of conductor including an additional layer thereon to form adjacent conductive lines, depositing dielectric layer thereon and planarizing the dielectric layer. The removal of the additional layer if desired is also shown. See Figs. 30A-30B, 33A-33J, column 28 lines 38-68, column 31 line 33 to column 32 line 68. The additional layer employed is not limited to non-conductive materials and is presumed to be conductive and further encompasses conductive materials such as polysilicon, carbon, titanium nitride and their interchangeability and selection of suitable conventional conductive materials would have bee within the purview of one skilled in the art. Kodera et al. lack anticipation primarily in that the dielectric is not explicitly recited to be less than 3.6 or to be PTFE and the space below adjacent conductor is not explicitly recited.

Jeng '493 teaches the use of low dielectric constant material, e.g., organic polymer such as polytetrafluoroethylene, column 3 lines 48-52, between interconnect lines to reduce line-to-line capacitance, crosstalk, power dissipation, RC time delay. The provision of the material between the conductive lines followed by etchback is also taught. Subsequent dielectric deposition and planarization is also taught. See column 1 line 30 to column 2 line 15, column 3 line 29 to column 5 line 43.

Jeng '303 also teach the problem of RC delayer, power dissipation, crossstalk due to dielectric having high dielectric constant, e.g., column 1 lines 37-63, and further

teach the use of low k dielectric between the stacks, e.g., as in Fig. 8-10, column 2 lines 37-38, column 3 lines 12-47, column 4 lines 48-61.

Shih et al. teach spaces 24 between conductor pattern 15 extending below a lower surface of the conductor 15. The advantages include the removal of any residues between adjacent electrodes thereby preventing shortage. See the abstract, Figs. 6-7, column 1 line 33 to column 2 line 2, column 3 lines 38-41. The prior art process of provision of spaces below the wiring, e.g., 18, is also shown in Fig. 1C column 1 lines 42-61.

It would have been obvious to one skilled in the art at the time the invention was made in practicing the Kodera et al. process to have employed low dielectric constant materials including below 3.6 such as polytetrafluoroethylene between interconnect lines as taught by Jeng '493 and 'Jeng '303 since such is conventional and advantageous as evidenced by Jeng. Etchback for planarization is conventional as evidenced by Jeng and further is a well-known alternative to chemical mechanical polishing and as such would have been obvious. The planarization of the upper insulating is well known in the art as evidenced by Jeng and enables a planarized top insulating surface to be obtained. The use of various alternative conductive materials, is well within the purview of one skilled in the art and as such would have been obvious.

It would have been further obvious to one skilled in the art in practicing the above invention to have included effected the etching patterned the adjacent wiring the space below the lower surface of adjacent wirings since such is conventional in the art as evidenced in Shih et al. to remove residue or nodules thereby preventing shortage

between adjacent electrodes. The dielectric having lower surface below lower surface of adjacent conductive lines would follow when such overetch is employed as suggested by Shih et al. Regarding the fringe capacitance recited in certain claims, e.g., claims 35-38, to the extent such is required to any specified or sufficient extent, such would be realized or result when the dielectric is situated above or below the surface of the adjacent conductive lines and further would follow when low dielectric constant material is employed.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-32 of U.S. Patent No. 6,107,183. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant claims would have been obvious over the claims in '183 wherein the additional layer in the instant claims correspond to the electrically conductive additional layer in '183 and wherein the low dielectric constant would have been inherent when PTFE or otherwise would have been conventional and

obvious as delineated above, e.g., as in Jeng. Regarding the amended feature of the space between adjacent metal lines below lower surface such would have been conventional and obvious to ensure removal of residues or nodules between the adjacent wirings as delineated above.

Applicant's arguments filed September 4, 2002 have been fully considered but they are not persuasive.

Initially with regard to the fringe capacitance delineated in claims 35-38, see the new grounds delineated above. Insofar as previous response remains applicant, they are repeated below. Applicant argues that the prior art does not address the problem of the fringe capacitance. The claims nonetheless are not limited to and are silent regarding any fringe capacitance. In addition, see the teachings above in Shih et al. wherein the overetching of the conductor pattern is conventional to ensure removal of any residue between the adjacent wirings thereby preventing any shortage. It remains apparent that such overetch is well within the purview of one skilled in the art and is conventional to ensure complete etching of the conductor patterns and to ensure removal of any residues therebetween. The provision of the low-K dielectric materials between the adjacent wirings is well known in the art as evidenced by either Jeng. The well-known advantages include the reduction of capacitance, crosstalk, power dissipation, RC time delay which are enumerated. The advantage of fringe capacitance to the extent realized would also follow the prior art process and in any event, is not the sole issue and does not outweigh the various advantages taught by the prior art as delineated above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Quach whose telephone number is 703-308-1096. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan Quach
Primary Examiner